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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/903,239	07/11/2001	Delbert Raymond Cecchi	ROC920010130US1	9489

7590 10/05/2004

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EXAMINER	
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ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/903,239
Filing Date: July 11, 2001
Appellant(s): CECCHI ET AL.

Bryan W. Bockhop
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 7/29/04.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1-10 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6429685	Stockstad	08-2002
6313696	Zhang	11-2001
5703532	Shin et al.	12-1997
5039873	Sasaki	08-1991
4958133	Bazes	09-1990

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (USP 6,313,696) in view of Sasaki (USP 5,039,873). This rejection is set forth in a prior Office Action, mailed on 03/05/04.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (USP 6,313,696) in view of Sasaki (USP 5,039,873).

With respect to claim 1, Figure 2 of the Zhang reference discloses a differential amplifier which includes: an active differential amplification circuit (transistors 31, 34, 41-46, 38, and 35 in Figure 2) electrically coupled to a first input signal (ina), a second input signal (inb) and an output signal (out), the active differential amplification circuit (transistors 31, 34, 41-46, 38, and

35) also electrically coupled to a first voltage (Vdd) and a second voltage (GND) different from the first voltage (Vdd); and a bias circuit (transistors 32, 33, 36 and 37 in Figure 2) electrically coupled to the active differential amplification circuit (transistors 31, 34, 41-46, 38, and 35) for biasing the active differential amplification circuit (transistors 31, 34, 41-46, 38, and 35). The Zhang reference does not teach that the bias circuit (transistors 32, 33, 36 and 37) is a passive circuit. However, the Sasaki reference teaches that when a transistor is on, it is functionally equivalent to a resistor (see Figure 4c, and Col. 1, lines 21-22 of Sasaki). Therefore, because each of the gates of the transistors 32, 33, 36 and 37 of the bias circuit in Figure 2 of the Zhang reference is connected to a respective fixed power supply voltage (Vdd or Gnd) so transistors 32, 33, 36 and 37 will remain on during switching (Col. 7, lines 37-41 of Zhang), it would have been obvious to one having an ordinary skill in the art at the time the invention was made to substitute a resistor for each of the transistors 32, 33, 36 and 37 in Figure 2 of the Zhang reference because they are functionally equivalent and because it is well known in the art that the impedance of the passive resistor is inherently linear (evidence is shown in Col. 5, lines 20-21 of the Stockstad reference, USP 6,429,685) and therefore, the use of passive resistor will improve overall linearity of the amplifier. With such a modification, the bias circuit will be a passive bias circuit which includes four resistors. Note that this modification will also meet the functional language "for providing common-mode rejection while providing differential-mode amplification" on lines 1-2 and "the active differential ... the second input signal" on the last 4 lines of the claim because the structure of the modification is the same as the structure of the claimed invention (Figure 2).

With respect to claim 2, the above modification shows that the active differential amplification circuit (transistors 31, 34, 41-46, 38, and 35 in Figure 2 of Zhang) includes: a first

transistor (34) having a first source electrically coupled to the first voltage (Vdd), a first gate electrically coupled to a first node (58) and a first drain (connected to node 52), the first node (58) being a bias node; a second transistor (31) having a second drain (connected to node 50), a second gate electrically coupled to the first node (58) and a second source electrically coupled to the second voltage (GND) different from the first voltage (Vdd); a third transistor (38) having a third source electrically coupled to the first voltage (Vdd), a third drain (connected to node of 56) and a third gate electrically coupled to the first node (58); a fourth transistor (35) having a fourth drain (connected to node 54), a fourth gate electrically coupled to the first node (58) and a fourth source electrically coupled to the second voltage (GND); a fifth transistor (41) having a fifth source electrically coupled to the first voltage (Vdd), a fifth drain electrically coupled to a second node (the junction of transistors 41-43) and a fifth gate electrically coupled to the first node (58); a sixth transistor (44) having a sixth drain electrically coupled to a third node (junction of transistors 44-46), a sixth gate electrically coupled to the first node (58) and a sixth source electrically coupled to the second voltage (GND); a seventh transistor (42) having a seventh source electrically coupled to the second node (junction of transistors 41-43), a seventh drain electrically coupled to the second drain (the connection of transistors 42 and 31 at node 50), and a seventh gate electrically coupled to the first input signal (ina); an eighth transistor (45) having an eighth drain electrically coupled to the first drain (the connection of transistors 45 and 34 at node 52), an eighth source electrically coupled to the third node (junction of transistors 44-46) and an eight gate electrically coupled to the first input signal (ina); a ninth transistor (43) having a ninth source electrically coupled to the second node (junction of transistors 41-43), a ninth gate electrically coupled to the second input signal (inb) and a ninth drain electrically coupled to the

fourth drain (the connection of transistors 43 and 35 at node 54); and a tenth transistor (46) having a tenth drain electrically coupled to the third drain (the connection of transistors 46 and 38 at node 56), a tenth gate electrically coupled to the second input signal (inb) and a tenth source electrically coupled to the third node (junction of transistors 45-46).

With respect to claim 3, the above modification also meet the limitation that the passive bias circuit includes: a first resistor (substituted for transistor 33 as discussed above with regard to claim 1) electrically coupling the first drain (node 52) to the first node (58); a second resistor (substituted for transistor 32 as discussed above with regard to claim 1) electrically coupling the second drain (node 50) to the first node (58); a third resistor (substituted for transistor 37 as discussed above with regard to claim 1) electrically coupling the third drain (node 56) to the output signal (out); and a fourth resistor (substituted for transistor 36 as discussed above with regard to claim 1) electrically coupling the fourth drain (node 54) to the output signal (out).

With respect to claim 4, Figure 2 of the Zhang reference shows that the first transistor (34), the third transistor (38), the fifth transistor (41), the seventh transistor (42) and the ninth transistor (43) each include a p-channel device.

With respect to claim 5, Figure 2 of the Zhang reference shows that the second transistor (31), the fourth transistor (35), the sixth transistor (44), the eighth transistor (45) and the tenth transistor (46) each include an n-channel device.

With respect to claim 6, Figure 2 of the Zhang reference shows that second voltage (GND) is electrically coupled to a common ground (GND).

With respect to claim 7, the above modification of Figure 2 of the Zhang reference as discussed in claim 1 also meets all of the limitations of claim 7 because the structure of this

modification is the same as the structure of the claimed invention (Figure 2), e.g., the above modification is a differential amplifier which includes: a first transistor (34) having a first source electrically coupled to the first voltage (Vdd), a first gate electrically coupled to a first node (58) and a first drain (connected to node 52), the first node (58) being a bias node; a second transistor (31) having a second drain (connected to node 50), a second gate electrically coupled to the first node (58) and a second source electrically coupled to a second voltage (GND) different from the first voltage (Vdd); a first resistor (substituted for transistor 33 as discussed above with regard to claim 1) electrically coupling the first drain (node 52) to the first node (58); a second resistor (substituted for transistor 32 as discussed above with regard to claim 1) electrically coupling the second drain (node 50) to the first node (58); a third transistor (38) having a third source electrically coupled to the first voltage (Vdd), a third drain (connected to node of 56) and a third gate electrically coupled to the first node (58); a fourth transistor (35) having a fourth drain (connected to node 54), a fourth gate electrically coupled to the first node (58) and a fourth source electrically coupled to the second voltage (GND); a third resistor (substituted for transistor 37 as discussed above with regard to claim 1) electrically coupling the third drain (node 56) to an output signal (out); and a fourth resistor (substituted for transistor 36 as discussed above with regard to claim 1) electrically coupling the fourth drain (node 54) to the output signal (out); a fifth transistor (41) having a fifth source electrically coupled to the first voltage (Vdd), a fifth drain electrically coupled to a second node (the junction of transistors 41-43) and a fifth gate electrically coupled to the first node (58); a sixth transistor (44) having a sixth drain electrically coupled to a third node (junction of transistors 44-46), a sixth gate electrically coupled to the first node (58) and a sixth source electrically coupled to the second voltage

(GND); a seventh transistor (42) having a seventh source electrically coupled to the second node (junction of transistors 41-43), a seventh drain electrically coupled to the second drain (the connection of transistors 42 and 31 at node 50), and a seventh gate electrically coupled to a first input signal (ina); an eighth transistor (45) having an eighth drain electrically coupled to the first drain (the connection of transistors 45 and 34 at node 52), an eighth source electrically coupled to the third node (junction of transistors 44-46) and an eight gate electrically coupled to the first input signal (ina); a ninth transistor (43) having a ninth source electrically coupled to the second node (junction of transistors 41-43), a ninth gate electrically coupled to a second input signal (inb) and a ninth drain electrically coupled to the fourth drain (the connection of transistors 43 and 35 at node 54); and a tenth transistor (46) having a tenth drain electrically coupled to the third drain (the connection of transistors 46 and 38 at node 56), a tenth gate electrically coupled to the second input signal (inb) and a tenth source electrically coupled to the third node (junction of transistors 45-46). Note that the preamble recitation "for providing common-mode rejection while providing differential-mode amplification" on lines 1-2 is merely intended use.

With respect to claim 8, Figure 2 of the Zhang reference shows that the first transistor (34), the third transistor (38), the fifth transistor (41), the seventh transistor (42) and the ninth transistor (43) each include a p-channel device.

With respect to claim 9, Figure 2 of the Zhang reference shows that the second transistor (31), the fourth transistor (35), the sixth transistor (44), the eighth transistor (45) and the tenth transistor (46) each include an n-channel device.

With respect to claim 10, Figure 2 of the Zhang reference shows that second voltage (GND) is electrically coupled to a common ground (GND).

(11) Response to Argument

Appellant argues on pages 4 of the brief (last 8 lines of the page) that there is no suggestion or motivation to combine the Zhang reference with the Sasaki reference to achieve the claimed invention. However, this argument is not persuasive because the motivation/suggestion was provided as the advantage of the passive resistor is that the passive resistor is inherently linear (evidence is shown in Col. 5, lines 20-21 of the Stockstad reference, USP 6,429,685). Therefore, the use of the passive resistor will improve overall linearity of the amplifier.

In response to appellant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning (3rd paragraph of page 5 to 1st paragraph of page 6 of the brief), it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Specifically, because each of the gates of the transistors 32, 33, 36 and 37 of the bias circuit in Figure 2 of the Zhang reference is connected to a respective fixed power supply voltage (the gate of p-channel transistors 33 and 37 connected to ground, and the gate of n-channel transistors 32 and 36 connected to power supply Vdd) so transistors 32, 33, 36 and 37 will remain on during switching (see Col. 7, lines 37-41 of Zhang), so each of the transistors 32, 33, 36 and 37 functions as a resistor since the Sasaki reference teaches that when a transistor is on, it is functionally equivalent to a resistor (see Figure 4c, and Col. 1, lines 21-22 of Sasaki).

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the invention to replace each of the transistors 32, 33, 36, and 37 with a passive resistor because they are functionally equivalent, and provide the advantage of improving the linearity of the amplifier.

Appellant next argues (2nd paragraph, page 6 of the brief) that "the asserted equivalence shown in Sasaki only indicates that a FET in a microwave signal switching circuit behaves like a resistor under certain conditions, not that a FET may be replaced by a resistor in an amplifier". However, this argument is not persuasive because the Sasaki reference discloses that when a transistor is on, it is functionally equivalent to a resistor (see Figure 4c, and Col. 1, lines 21-22 of Sasaki), and because each of the gates of the transistors 32, 33, 36 and 37 of the bias circuit in Figure 2 of the Zhang reference is connected to a respective fixed power supply voltage (the gate of p-channel transistors 33 and 37 connected to ground, and the gate of n-channel transistors 32 and 36 connected to power supply Vdd) so transistors 32, 33, 36 and 37 will remain on during switching (see Col. 7, lines 37-41 of Zhang), so each of the transistors 32, 33, 36 and 37 functions as a resistor since the Sasaki reference teaches that when a transistor is on, it is functionally equivalent to a resistor.

Appellant further argues (3rd paragraph, page 7 of the brief) that "Sasaki does not teach that a resistor is a functional equivalent to an always-on FET, but only that an always-on FET can be modeled as a resistor under certain conditions. In the environment of the amplifier discloses in Zhang, a transistor would not act in the same way that a passive resistor would". However, the Sasaki reference clearly discloses that when a transistor is on, it is functionally equivalent to a resistor (see Figure 4c, and Col. 1, lines 21-22 of Sasaki). The Sasaki reference

does not state any condition that an ON-FET is not function as a resistor. Therefore, when a transistor is ON, it is functionally equivalent to a resistor.

Appellant further argues (2nd and 3rd paragraphs, line 8 of the brief) that "the FET-resistor equivalence model shown in Fig. 4(c) of Sasaki is valid only when a FET is operating with a gate-to-source voltage (V_{GS}) that is held substantially constant, and then it is useful model only so long as the drain-to-source voltage (V_{DS}) is maintained within a narrow range". However, the Sasaki reference does not specially stated that the gate-to-source voltage V_{GS} must be constant and that the drain-to-source voltage V_{DS} must be maintained within a narrow range. Clearly, the Sasaki reference shows in Figure 4c and line 20-21 of Col. 1 that when a FET is ON, it is equivalence as a resistor. The Sasaki reference does not state any specific condition that an ON-FET is not function as a resistor. Therefore, when a transistor is ON, it is functionally equivalent to a resistor.

Appellant further argues (last line of 2nd paragraph, page 8 of the brief) that "a resistor is not a functional equivalent of a FET when used as biasing transistor in a differential amplifier". However, this argument is not persuasive because each of the gates of the transistors 32, 33, 36 and 37 of the bias circuit in Figure 2 of the Zhang reference is connected to a respective fixed power supply voltage (the gate of p-channel transistors 33 and 37 connected to ground, and the gate of n-channel transistors 32 and 36 connected to power supply Vdd) so transistors 32, 33, 36 and 37 will remain on during switching (see Col. 7, lines 37-41 of Zhang). Since these transistors are ON, each of these transistors 32, 33, 36 and 37 must be functionally equivalent to a resistor.

Appellant further argues (1st paragraph of page 9 of the brief) that the Stockstad reference serves only to further contrast a FET from a linear resistor and demonstrates the inadequacy of the equivalence model disclosed in Sasaki. In response, the Stockstad reference was cited to support the notoriously well-known fact that passive resistor function in a linear manner (line 20-21 of Col. 5).

Appellant further argues (3rd paragraph of page 9 and 1st and 2nd paragraphs of page 10 of the brief) that the analysis performed by Mr. Preuss (comparing the result of the circuit with the source-drain resistance of a biasing FET of the Zhang amplifier, and the circuit which has the resistance of a resistor put in place of this FET (namely, the invention)) which indicates that the relevant transistors from Figure 2 of Zhang do not behave linearly as passive resistors. However, this argument is not persuasive because the claim was not rejected under 102 so the circuits cannot be compared. Because the claims are rejected under 35 U.S.C. 103, the circuit in Zhang can only be compared after the circuit in Zhang is modified. Note that, by modifying the amplifier of Zhang as discussed (i.e., each of the transistors M13, M12, M8, and M9 in Figure 2 of Zhang is replaced by a passive resistor which is discussed in the above 103 rejection), then the modification circuitry would be identical to the applicant's invention and then the modification circuitry will perform identical as applicant's invention.

Appellant further argues (2nd paragraph, page 10 of the brief) that the Sasaki equivalent mode makes no mention of any capacitance in the FET and that the FET includes gate-to-drain, gate-to-base, drain-to-base, and source-to-base capacitances, and that these capacitances introduce importance delays in differential amplifier. However, this argument is not persuasive because the claims are not rejected under 35 U.S.C. 102. Instead, the claims are rejected under

35 U.S.C. 103, and that when each of the biasing transistors M13, M12, M8, and M9 in Figure 2 of Zhang is replaced by a resistors (as discussed in the 103 rejection) then the concern regarding the capacitance would be irrelevant.

Appellant further argues (2nd paragraph of page 11 to 1st paragraph of page 12 of the brief) that "none of the office actions include any indication that there is a suggestion of the desirability to combine Sasaki with Zhang". However, this argument is not persuasive because the office action suggested that to replace each of the biasing transistors with a passive resistor because the passive resistor has an advantage that it is inherently linear. Thus, the overall linearly of the amplifier will be improved.

Applicant further argues (2nd paragraph, page 12 of the brief) that "In response to a challenge to produce documentary evidence of a suggestion of motivation to combine the reference under MPEP 2144.03(C), no such documentary evidence was provided". However, this argument is not persuasive because in the last office action (mailed on 3/5/04), the Examiner provided document to support that the advantage of using passive resistor because the impedance of passive resistor inherently is linear (evidence is shown in Col. 5, lines 20-21 of the Stockstad reference, USP 6,429,685; and by Ohm's law V = IR, one skill in the art also recognizes that the passive resistor is linearly).

Finally, Applicant argues (3rd and 4th paragraphs, page 12 of brief) that "it was not obvious to employ a passive resistor in a differential amplifier, thereby taking advantage of the linear property of the passive resistor" and that "nowhere in the record is there any indication that prior art "suggests the desirability of the combination" of a passive resistor with a differential amplifier". However, in response to applicant's argument that there is no suggestion

to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, because each of the gates of the transistors 32, 33, 36 and 37 of the bias circuit in Figure 2 of the Zhang reference is connected to a respective fixed power supply voltage (the gate of p-channel transistors 33 and 37 connected to ground, and the gate of n-channel transistors 32 and 36 connected to power supply Vdd) so transistors 32, 33, 36 and 37 will remain on during switching (see Col. 7, lines 37-41 of Zhang), so each of the transistors 32, 33, 36 and 37 functions as a resistor since the Sasaki reference teaches that when a transistor is on, it is functionally equivalent to a resistor (see Figure 4c, and Col. 1, lines 21-22 of Sasaki). Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the invention to replace each of the transistors 32, 33, 36, and 37 with a resistor because they are functionally equivalent and that the advantage of using passive resistor because the impedance of passive resistor inherently is linear (evidence is shown in Col. 5, lines 20-21 of the Stockstad reference, USP 6,429,685; and by Ohm's law V = IR, one skill in the art also recognizes that the passive resistor is linearly), and thus the use of passive resistor will improve overall linearity of the amplifier.

(11) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Examiner Long Nguyen
September 20, 2004

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